REMARKS

This is in full and timely response to the non-final Office Action dated February 6, 2004. Reexamination in light of the following remarks is respectfully requested.

Claims 1-15 are currently pending in this application, with claims 1, 3 and 5 being independent. No new matter has been added.

Rejection Under 35 U.S.C. §102

Claims 1-6 were rejected under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,448,953 to Murade.

This rejection is respectfully traversed for at least the following reasons.

Claim 1 and the claims dependent thereon include the features of:

a pixel part comprised of pixels arranged in a matrix and having a signal line arranged for each pixel string,

a clock generating means for generating a first clock signal and a first inverse clock signal having inverse phases to each other and serving as a reference for horizontal scanning and generating a second clock signal and a second inverse clock signal having the same period and having a smaller duty ratio than the first clock signal and said first inverse signal based on said first clock signal and said first inverse clock signal,

a shift register for performing a shift operation in synchronization with said first clock signal and said first inverse clock signal outputting a shift pulse in sequence from the shift stages,

a first switch group for sampling said second inverse clock signal or said second clock signal in response to a shift pulse output in sequence from said shift register, and

a second switch group for sampling an input video signal in sequence in response to said second inverse clock signal or said second clock signal sampled by the switches of the first switch group and supplying the sampled input video signal to the signal lines of the pixel part, wherein:

said second switch group samples the input video signal in response to said second inverse clock signal and supplies the sampled input video signal to said signal lines arranged in the odd columns, and samples the input video signal in response to said second clock signal and supplies the sampled input video signal to said signal lines arranged in the even columns.

Claim 3 and the claims dependent thereon include the steps of:

generating a second clock signal and said second inverse clock signal having the same period and having a smaller duty ratio than the first clock signal and the first inverse clock signal based on the first clock signal and the first inverse clock signal,

sampling the second inverse clock signal and the second clock signal based on the shift pulse, and

supplying the video signal to signal lines arranged in odd columns of the pixel part while sampling the video signal by the second inverse clock signal and supplying the video signal lines arranged in even columns of the pixel part while sampling the video signal by the second clock signal.

Claim 5 and the claims dependent thereon include the features of:

a clock generating means for generating a first clock signal and a first inverse clock signal having inverse phases to each other and serving as a reference for horizontal scanning and generating a second clock signal and a second inverse clock signal having the same period and having a smaller duty ratio than the first clock signal and said first inverse signal based on said first clock signal and said first inverse cloak signal,

a display panel having a pixel part comprised by pixels arranged in a matrix and having a signal line arranged for each pixel string and a horizontal driving system for sampling said second inverse clock signal and said second clock signal based on a shift pulse obtained in sequence in synchronization with said first clock signal and said first inverse clock signal and sampling an input video signal in sequence in response to said sampled second inverse clock signal and said second clock signal and supplying the sampled input video signal to the signal lines of the pixel part, wherein said display panel samples the input video signal in response to said second inverse clock signal and supplies the sampled input video signal to the signal lines arranged in the odd columns, and samples the input video signal in response to said second clock signal and supplies the sampled input video signal to the signal lines arranged in the even columns,

an emitting means for emitting light to said display panel, and

a projecting means for projecting light passing through the display panel to a screen.

"A claim is anticipated *only if* each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (emphasis added). *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Murade arguably teaches a driving circuit for electro-optical device, electro-optical device, and electronic apparatus having a first clock signal CLX, a first inverse clock signal CLX', a second clock signal ENB1, and a second inverse clock signal ENB2 (figure 4).

While Murade arguably teaches the second clock signal ENB1 and a second inverse clock signal ENB2 having the same period as the first clock signal CLX and the first inverse clock signal CLX', Murade fails to disclose, teach or suggest the second clock signal ENB1 and the second inverse clock signal having a smaller duty ratio than the first clock signal CLX and the first inverse clock signal CLX'.

Withdrawal of these rejections and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: July 6, 2004

Respectfully submitted,

By _____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant